**ECE 6101 Exam**

**Instructions:** You have 1 hour and 20 minutes to complete this exam. The exam is closed book and closed notes, with the exception of one 8.5x11 sheet. No calculators are allowed.

Problem 1

Problem 2

Problem 3

Problem 4

Problem 5

TOTAL
1) 20 points

Calculate the number of cycles required for the following cache coherence protocols:

   a) write-through coherence
   b) Dragon

on each of the following memory reference streams:

   i) r1 r2 r3 w1 w2 w3 r1 r2 r3
   ii) r1 w1 r2 w2 r3 w3 r4 w4

All of the references are to the same location: r/w indicates read or write, and the digit refers to the processor issuing the reference. Assume that all caches are initially empty, and use the following cost model: cache hit – 1 cycle; transfer of full cache block across bus – 50 cycles; all other bus transactions, e.g. write-thru, write-update, – 30 cycles.
2) 20 points

Implement a compare&swap operation in assembly language using LL-SC.
3) 20 points

Consider the below implementation of a barrier synchronization procedure. Whenever a process reaches a barrier point, it calls BARRIER(n), where n is the number of processes involved in the barrier. Assume n has the same value for each call to BARRIER. The variables releasing, count, and lock are global shared variables with initial values of false, zero, and unlocked, respectively. Functions acquire() and release() atomically acquire and release a lock.

```c
BARRIER(n)
{
    acquire(lock);
    count++;
    if (count == n) {
        releasing = true;
        count--;
    }
    else {
        release(lock);
        while (NOT releasing)
            NOP;
        acquire(lock);
        count--;
        if (count == 0) releasing = false;
    }
    release(lock);
}
```

a) This procedure is not guaranteed to work correctly on a sequence of barrier operations carried out by a group of processes. State the problem that makes the procedure incorrect.

b) Modify the code to fix the problem. Try to make the smallest possible modification that results in correct code.
4) 20 points

Consider an 8x8 Omega network. Call the time that it takes for 1 processor to read a memory module without contention a network cycle. This includes the time for the processor to connect to the memory module through the network, the time for the memory access to take place, and the time for the value to be sent back through the network to the processor. Assume the network is circuit-switched, i.e. a connection is maintained in the network continuously while a memory read is taking place. What is the minimum number of network cycles required to complete the following set of read requests that are all submitted simultaneously to the network? Show sufficient work to enable determination that your solution method is correct. You may want to draw the network to help you.

P0:M4  P1:M6  P2:M1  P3:M0  P4:M7  P5:M3  P6:M5  P7:M2
5) 20 points

What are the diameter and bisection width of a complete binary fat tree of height $h \geq 1$? Recall that in a fat tree the number of links between nodes is doubled at each level as you move up the tree. So, a leaf has 1 link to its parent, which has 2 links to its parent, which has 4 links to its parent, etc. Make sure to justify your answer.