1) 25 points

a) List a common atomic machine instruction that is used to support locks and mutual exclusion.

b) Name the technique that is used in vector processors to handle vectors of length greater than the size of the vector registers.

c) What is the primary difference between a fine-grain dataflow computer and a coarse-grain dataflow computer?

d) What type of switching produces a pipelined form of packet transmission?

e) Name two parallel programming models.

f) Define speedup in terms of $T_s$, the time to execute a program on a uniprocessor system, and $T_p$, the time to execute the same program on a multiprocessor system having the same type of processor.

g) How many switching elements does an nxn crossbar switch contain?
h) What type of parallel computer is dedicated to performing a specialized computation by pulsing data through an interconnected set of simple computational cells?

i) List two features of the SGI Challenge’s Powerpath-2 bus that contribute to its high bandwidth.

j) What are two key aspects of the Sun E10000 server architecture that allow it to scale well with the number of processors while maintaining a simple cache coherence mechanism?

k) Which of the networks we studied during the semester is the most similar to IBM SP’s High-Performance Switch network?

l) State the function of the reduction network present in the MasPar MP-1.
2) 15 points

a) Write an MPI program segment that runs on at least two processes and definitely causes the program to deadlock. Do not worry about listing every parameter for the MPI calls that you use. Rather, list only the critical parameters and indicate their meaning.

b) State two different ways in which you can modify your program to eliminate the deadlock.
3) 15 points

Consider a vector operation that requires 20 clock cycles to set up and which is executed in a 40-stage pipeline.

a) Evaluate the speedup obtained for vector lengths of 32, 64, 128, and 256. Justify your answers.

b) What is n_{1/2} for this operation? Justify your answer.
4) 15 points
Consider the following MPI program segments running on two processes, 0 and 1 (assume comm is set to a group containing only processes 0 and 1, and tag is equal on the two processes):

Process 0

N = 15;
MPI_Send(&N, 1, MPI_INTEGER,
         1, tag, comm, &stat);
MPI_Barrier(comm);

Process 1

MPI_Irecv(&R, 1, MPI_INTEGER,
          0, tag, comm, &stat);
MPI_Barrier(comm);
Calc_function(R);

Will Calc_function(R) calculate the correct value in this program? Why or why not? If not correct, modify the program to fix it.
5) 15 points

Consider an 8-processor SIMD computer with distributed memory and a bi-directional ring network connecting the processors.

a) Describe an algorithm using *add*, *multiply*, and *route* instructions to compute the expression

\[ s = (A_1 \times B_1) + (A_2 \times B_2) + \cdots + (A_{32} \times B_{32}) \]

in the minimum time possible. Assume add instructions take 1 cycle, multiply instructions take 2 cycles, and route instructions take 1 cycle. Memory access time is ignored. Assume operands \( A_i \) and \( B_i \) are initially stored in \( P_{i \mod 8} \). A route instruction involves passing a single data item to either the left or right neighbor.

b) What is the minimum time to compute the expression? Justify your answer.
6) 15 points

Consider a vector processor with a single memory pipeline and having the following parameters:

- add start-up cost = 6 cycles
- dependence penalty = 4 cycles
- memory access time = 12 cycles
- vector register size = 64

and consider the following code run with fixed vectors of length 64:

```plaintext
LV V1, Ra
LV V2, Rb
ADDV V3, V2, V1
SV Rc, V3
```

a) Assuming no chaining, how many clock cycles does this code require? Justify your answer.

b) With chaining, how many clock cycles are required? Justify your answer.