ECE 3055C Quiz I

1) 25 points

Consider the execution of a sequence of 1000 MIPS instructions. Assume that 100 of the instructions are branches, 200 are load words, and the rest are register-to-register or store word instructions.

Calculate the speedup that is achieved by a pipelined datapath versus a multi-cycle datapath on this sequence of instructions with the following assumptions:
- The clock cycles for both datapaths are 2 ns.
- For the multi-cycle datapath, load word instructions take 5 cycles, branches take 3 cycles, and all other instructions take 4 cycles.
- The pipelined datapath uses the forwarding scheme described in Chapter 6 of Patterson and Hennessy, but does not do branch prediction. Any hazards not removed by the forwarding hardware are handled by the compiler, which does not perform any optimizations.

State any additional assumptions that you make in your speedup calculation.
2) 25 points

Consider the following MIPS assembly program executing on a pipelined datapath with no hardware for hazard handling. Assume a branch penalty of 2 cycles.

Loop:  
\begin{align*}
\text{add} & \quad $1, $2, $3 \\
\text{sub} & \quad $4, $5, $1 \\
\text{or} & \quad $5, $6, $7 \\
\text{and} & \quad $8, $9, $10 \\
\text{slt} & \quad $11, $12, $5 \\
\text{beq} & \quad $13, $14, \text{Loop} \\
\text{add} & \quad $15, $16, $17
\end{align*}

a) Add as few NOPs as possible to this instruction sequence to ensure that hazards are eliminated and the code executes correctly. Do not reorder any instructions.

b) Now reorder the instructions to eliminate as many NOPs as possible without affecting the correctness of execution.
3) 25 points

Consider the pipelined datapath with control shown below and taken from Chapter 6 of Patterson and Hennessy. Assume the control signals at EX, MEM, and WB stages have the following values, where the left-most bit corresponds to the upper-most bit in the figure:

- EX: 100001100
- MEM: 11010
- WB: 00

Based on the values of the control signals, state what instructions are executing in each of these stages. If you cannot identify an instruction exactly, narrow the instruction down to the smallest set of possibilities. Recall that the only instructions implemented by this datapath are lw, sw, add, sub, and, or, slt, beq.
4) 25 points

Consider the following MIPS code executing on the pipelined datapath with forwarding shown below. The A and B inputs of the ALU can come from the register file, EX/MEM.ALUResult, or write_data (the output of the WB-stage MUX). The B input can also come from ID/EX.SignExtend for immediate data. For each instruction, state from which of these places the A and B inputs of the ALU come when that instruction is in the EX stage.

Loop: add $1, $2, $3
     sw $4, 0($1)
     or $6, $4, $1
     slt $6, $3, $5
     and $0, $6, $1
     beq $0, $0, Loop