ECE 3055 - Homework #2 Solutions

40-bit virtual addresses
24-bit physical addresses
page size = 16 KB

@ 1-level page table

#entries = # virtual pages = \( \frac{2^{40} \text{ bytes in addr. space}}{2^{14} \text{ bytes/page}} \)

# entries = \( 2^{26} \)

each entry contains page frame #, valid bit, dirty bit
#bits for page frame # = 24-14 = 10

\( \therefore \) each entry needs 12 bits or 2 bytes

\[ \therefore \text{size of page table} = 2^{27} \text{ bytes} = 128 \text{ MB} \]

(Note: this is larger than the physical memory)

@ Root table has 1 entry per page of 2nd level table, which is same size as the 1-level table

#entries = # pages in 2nd level table = \( \frac{2^{27}}{2^{14}} = 2^{13} \)

entry size is same as in @, i.e. 2 bytes

\( \therefore \text{size of root page table} = 2^{14} \text{ bytes} = 16 \text{ KB} \)

(Note: page table fits in 1 page)
#### Inverted Page Table

\[
\text{# entries} = \text{# page frames} \times 2 = \frac{2^{24}}{2^{14}} \times 2 = 2^{10}
\]

Each entry contains pid, virtual page #, page frame #, valid bit, dirty bit, pointer.

- Each entry is 58 bits or 8 bytes.

- Size of inverted table = \(2^{14}\) bytes = 16 KB

(Note: page table again fits in 1 page)

#### 16-entry Direct-mapped TLB

16-bit virtual addresses \(\rightarrow\) virtual addresses are 12-bit physical addresses

Page size = 256 bytes

<table>
<thead>
<tr>
<th>Address</th>
<th>Hit/Miss</th>
<th>Phys. Address</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>00013</td>
<td>M</td>
<td>213</td>
<td>00 (\rightarrow) TLB</td>
</tr>
<tr>
<td>022CF</td>
<td>M</td>
<td>ACF</td>
<td>22 (\rightarrow) TLB</td>
</tr>
<tr>
<td>03A1</td>
<td>H</td>
<td>EA1</td>
<td>none</td>
</tr>
<tr>
<td>0101</td>
<td>M</td>
<td>FO1</td>
<td>01 (\rightarrow) TLB</td>
</tr>
<tr>
<td>00FF</td>
<td>H</td>
<td>2FF</td>
<td>none</td>
</tr>
<tr>
<td>3115</td>
<td>M</td>
<td>C15</td>
<td>21 (\rightarrow) TLB</td>
</tr>
<tr>
<td>2266</td>
<td>H</td>
<td>A66</td>
<td>none</td>
</tr>
</tbody>
</table>
TLB final contents:

<table>
<thead>
<tr>
<th>Block</th>
<th>Tag</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>C</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>E</td>
</tr>
</tbody>
</table>

Case 1: TLB hit, cache hit

# cycles = 1

frequency = \(0.9 \times 0.95 = 0.855\)

Case 2: TLB hit, cache miss

# cycles = 1 + 30 + 1 = 32

frequency = \(0.9 \times 0.05 = 0.045\)

Case 3: TLB miss, cache hit

avg. # of mem. cycles for TLB miss = \(0.75 \times 30 + 0.25 \times 60\)

= 37.5
avg. # of cycles for Case 3 = 1 + 37.5 + 1 = 39.5

frequency = (0.1) x (0.95) = 0.095

Case 4: TLB miss, cache miss

avg. # of cycles = \( \frac{1}{3} + 37.5 + \frac{1}{3} + 30 + \frac{1}{3} = 70.5 \)

frequency = (0.1) x (0.05) = 0.005

Avg. # of cycles overall

= (1 x 0.855) + (3.2 x 0.045)
  + (39.5 x 0.095) + (70.5 x 0.005)

Avg. # cycles = 6.4